REMARKS

Claims 1-3, 5-10, and 12-14 are all the claims pending in the present application, new claims 12-14 having been added as indicated herein. The Examiner continues to reject claims 1-3, 5-7, 9 and 10 under 35 U.S.C. § 102(b) as allegedly being anticipated by Hanselmann, "Real-Time Simulation Replaces Test Drives," Test and Measurement World, February 15, 1996, pages 35-36, 38, and 40. Claim 8 continues to stand rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by Hanselmann in view of Turner (US Patent No. 6,269,020). The Examiner also adds new rejections under 35 U.S.C. § 112, first and second paragraph.

§ 112, first paragraph, Rejections - Claims 1-3 and 5-10

Applicant amends claim 1, as indicated herein, and believes that the Examiner's rejections of claims 1-3 and 5-10 under 35 U.S.C. § 112, first paragraph, are obviated.

§ 112, second paragraph, Rejections - Claims 8 and 10

The Examiner rejects claims 8 and 10 under 35 U.S.C. § 112, second paragraph, based on the reasons set forth on page 3 of the Office Action.

Applicant amends claim 8 and 10, as indicated herein, and believes that the Examiner's rejections of claims 8 and 10 under 35 U.S.C. § 112, second paragraph, are obviated.

§ 102(b) Rejections (Hanselmann) - Claims 1-3, 5-7, 9, and 10

The Examiner rejects claims 1-3, 5-7, 9, and 10 based on the reasons set forth on pages 5-11 of the Office Action.

In the *Response to Arguments* section of the present Office Action on pages 10-11, the Examiner states that based on the broadest reasonable interpretation, any output signal is qualified as a "low output signal," and therefore "all signals disclosed in [the] Hanselmann

reference" allegedly meet the claimed "low output signals." Based on this interpretation, the Examiner maintains the previous prior art rejections of the claimed invention. However, independent claim 1 is amended, as indicated herein, for clarification purposes, and Applicant believes that based on this clarification, the arguments set forth previously, and the arguments set forth below, Hanselmann does not anticipate claim 1.

Further to Applicant's previously submitted arguments, Applicant submits that Hanselmann does not disclose or suggest at least, "sending simulated input signals to said unit and receiving slow output signals from said unit in response to said simulated input signals by at least one microprocessor," and "receiving fast output signals in response to said input simulation signals by at least one programmable logic circuit," as recited in claim 1. That is, the operations set forth above, according to an exemplary embodiment of the present invention as recited in claim 1, can be performed by a microprocessor 14 and a logic circuit 18. The microprocessor 14 is adapted to receive and to process slow signals received from the unit under test 1. The logic circuit 18 is able to generate parameter values and store them in a memory 19. The microprocessor 14 is adapted to access the stored parameter values in the memory 19 with a signal S'1 slower than the fast output signal S1.

The apparatus described in Hanselmann contains a multiple digital signal processor (DSPs), an I/O board and an interfacing circuitry (page 36, first column, 1st paragraph). The DDS board of Hanselmann contains a dual port memory and a DSP (page 36, third column, 2nd paragraph). However, Hanselmann does not disclose that the DDS board contains a programmable logic circuit.

To the contrary, exemplary embodiments of the present invention comprise a programmable logic circuit 18.

There are exemplary beneficial results of using a programmable logic circuit over a DSP. For example, a DSP as used in Hanselmann processes signals sequentially whereas the logical circuit as claimed in an exemplary embodiment of the present invention, can process N signals in parallel. A DSP as used in Hanselmann contains only one arithmetic logic unit which allows the processing of only one signal at once. To the contrary, a logic circuit 18 as used in an exemplary embodiment of the present invention can process a plurality of signals synchronously without damaging the frequency of the output signals. To realize this same function, a plurality of DSP synchronized in parallel would have to be used in Hanselmann.

Further, contrary to Hanselmann, in the simulator according to exemplary embodiments of the present invention, the frequency of the slow signal S2 and the access frequency of the microprocessor 14 to the memory 19 are lower than the frequency of the microprocessor 14.

At least based on the above, as well as previously submitted arguments, Applicant submits that Hanselmann does not satisfy at least the above-quoted features of claim 1, and, thus, does not anticipate claim 1.

With respect to independent claim 5, Applicant submits that this claim is patentable at least based on reasons similar to those set forth above with respect to claim 1, as well as based on the arguments set forth in the previously submitted Amendment.

Applicant submits that claims 2, 3, 6, 7, 9, and 10 are allowable at least by virtue of their respective dependencies from independent claims 1 and 5.

§ 103(a) Rejections (Hanselmann / Turner) - Claim 8

Applicant submits that dependent claim 8 is allowable at least by virtue of its dependency from independent claim 5. Turner does not make up for the deficiencies of Hanselmann.

New claims 12-14 are added, as indicated herein, to provide a varying scope of coverage. Applicant submits that new claims 12-14 are patentable at least by virtue of their dependencies from independent claim 1.

Support for new claim 12 can be found on page 1, lines 23 to 27 of the specification; the specification states that the control signals issued by the electronic unit must be positioned in time with the precision of microseconds to control electronic circuits of GTO and IGBT type. In page 7, lines 35 and 36, the specification recites that fast signals can be control signals for GTO and IGBT circuits. By combining these sentences, one skilled in the art would understand that fast signals must be positioned in time with the precision of microseconds. In other words, the sampling period of these signals is based on microseconds. By applying the Shannon principle, one skilled in the art would deduce that the period of the fast output signal is in the order of two or more microseconds.

Support for new claim 13 is based on the specification at page 3, lines 7 to 10, page 7, lines 25 to 28 and at page 8, lines 13 to 18. In page 5, lines 7 to 10 of the specification, it is described that the unit must be capable of responding to signals issued at any instant with the precision of microseconds. Since the electronic unit 1 has to process signals with the precision of microseconds, the logic circuit 18 which processes fast signal outputted from the electronic

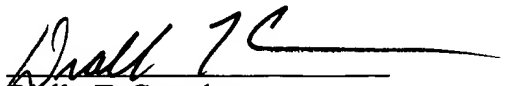
unit 1 has also to process signals with a precision of the microsecond order. In other words, the sampling period of these signals have to be in microseconds. So the first frequency is substantially equal to 1 mega Herz.

Support for new claim 14 is based on the specification at page 5, lines 5 and 6.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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